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Fabrication of Silicon Nanowires with Precise Diameter Control Using Metal Nanodot Arrays as a Hard Mask Blocking Material in Chemical Etching

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We report on a simple and cost-effective method to fabricate high density silicon nanowires (SiNWs) through catalytic chemical wet etching. Metallic chromium/gold (Cr/Au) nanodots were first deposited onto the silicon wafer using an anodic aluminum oxide (AAO) template. The AAO template was then removed before a thin blanket layer of gold catalyst was evaporated onto the sample surface. The gold-assisted chemical wet etching was carried out in a solution consisting of deionized water, hydrogen peroxide, and hydrofluoric acid to produce well-aligned silicon nanowires of uniform diameters. We demonstrate that the diameter of the silicon nanowires can be precisely controlled to a precision of 10 nm in the range of 40 to 80 nm through fine-tuning of the pore diameter of the AAO template. The reported fabrication procedure therefore gives a highly repeatable method to form well-aligned, uniform, and crystalline SiNWs of high density with controllable diameters below 100 nm. The use of Cr/Au as a hard mask blocking material will also be of great interest for the fabrication of other Si nanostructures using the catalytic etching process.

Introduction

Silicon nanowires (SiNWs) form an important group of one-dimensional nanostructures. The abundance of silicon (Si) as a material and the widespread use of its semiconducting properties make Si nanostructures extremely attractive for a wide range of applications. Much attention has been devoted to SiNWs as they have been regarded as an important platform for future technological revolution. The potential for applications of SiNWs has been demonstrated in areas of electronics,[1−3] optoelectronics,[4] sensors,[5] photovoltaics,[6,7] and thermoelectrics.[8,9] For both phenomenological studies and the implementation of practical applications of SiNWs, fabrication of regular arrays of Si wires, with precise control of the crystallographic orientation, dimension, and density will be of great value. The ability to achieve this fine control remains a key challenge in the fabrication of SiNWs.

A common technique for SiNW synthesis employs a catalytic tip-growth process based on the vapor−liquid−solid (VLS) mechanism[10] that has been proven to be versatile through nanowire growths from different techniques.[11−15] One limitation in the VLS technique, however, lies in the predominant axial growth orientation of the nanowires as only orientations of ⟨111⟩, ⟨112⟩, and ⟨110⟩ (depending on the wire diameters) are commonly observed.[16] Obtaining SiNWs in the ⟨100⟩ axial orientation by VLS is often difficult. While template-assisted VLS growth can provide the desired ⟨100⟩ direction,[17,18] the emphasis of the clean gold/silicon (Au/Si) interface may complicate matters, and it may be the reason why 10% of the observed pores did not achieve any wire growth. One possible alternative is to use deep reactive ion etching (DRIE) with a combination

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of nanoimprint lithography to produce regular SiNWs on Si (001) substrates.[19] However, the process is quite involved and there are often feature size dependent effects in this method.

On the contrary, synthesis of ⟨100⟩ SiNWs can be readily achieved through metal-assisted chemical wet etching,[20−22] which is a simple and cost-effective alternative that can produce wires of very high aspect ratios.[23] Briefly, an active metal, usually gold (Au) or silver (Ag) is used as a catalyst for etching of the underlying Si in a mixture of deionized (DI) water, hydrofluoric acid (HF), and hydrogen peroxide (H_2O_2). Nanostructures of different shapes and sizes can thus be fabricated based on the patterning of the metal catalyst, and this has been shown to be possible with laser interference lithography[24,25] and nanosphere lithography.[26] While these methods are relatively inexpensive and allow possible wafer-scale production of SiNWs, they may not be suitable for synthesis of nanowires with small diameters. Catalytic etching using nanosphere lithography has been demonstrated to give wires with diameter of ∼100 nm.[26] However, obtaining nanowires with diameters smaller than 100 nm may be difficult since there is a limitation in achieving reliable diameter reduction by reactive ion etching (RIE) for the smaller dimensions. For laser interference lithography, the ultimate achievable resolution equals to one-fourth of the laser wavelength.[27] This means that even for a deep UV wavelength of 200 nm, the smallest wire diameter obtainable is ∼50 nm. Though the diameter of the as-synthesized SiNWs can be further reduced controllably, through a simple post-growth oxidation-then-etching process, possibly down to a few nanometers,[28,29] the wire density, which is limited by the original wire inter-spacing, remains the same.

Another common patterning method employs the use of anodic aluminum oxide (AAO). This method is cheap and repeatable making it highly desirable for use as a mask for nanostructure synthesis since AAOs with a wide range of pore diameters and interpore distances can be fabricated. However, for the formation of SiNWs through catalytic etching, the surface exposed by the through pores of the AAO must be patterned as an inactive reaction layer. This is tricky as common blocking materials for etching such as photoresists cannot be easily patterned using the AAO. One way around the problem is to make use of RIE to pre-etch the hexagonal AAO pattern onto a Si (100) surface before the subsequent metal deposition and chemical wet etching. This has been demonstrated for the synthesis of SiNWs with diameters of 10 nm or less.[30] When a layer of Au or Ag was deposited onto the patterned and etched pores, the closure effect restricted the metal deposition at the bottom of the etched pores while the sidewalls of the pores received no coating at all. The rate of the chemical etching was found to be much faster on the top surface than that on the pore bottom since only a limited amount of metal (reported to be nanoparticles) was deposited at the pore bottom. This difference in the etch rates reportedly resulted in the formation of the SiNWs. While this is a useful approach for sub-10 nm diameter nanowires, the utilization of the closure effect for the self-assembly will put an upper limit on the achievable nanowire diameter. This is because to fabricate larger SiNWs, AAO masks with larger pores have to be used. The larger patterned and etched pores will significantly reduce the difference in coatings on the top, bottom, and side walls. The difference in the etch rates, which is the basis for the wires formation, may thus be insignificant. In this work, we report on an improved procedure whereby the AAO template can be used to form arrays of metal nanodots that act as a hard mask in fabricating SiNWs by chemical wet etching. Through the fine control over the pore size of the AAO template used in the metal dot deposition, we demonstrate the fabrication of uniform ⟨100⟩ SiNWs with high density and highly controllable diameters.

Experimental Details

Before describing our experimental procedure in detail, it is important to understand the mechanism behind the metal-assisted chemical etching in a solution containing HF and H_2O_2. In general, the formation of SiNWs by metal-assisted etching can be explained by a set of catalyzed reduction−oxidation or redox reaction. While the Si underneath the metal catalyst is oxidized, the counterpart reduction occurs for the H_2O_2. The HF present in the solution will subsequently dissolve the oxidized Si (SiO_x), thus allowing the redox reaction to continue. The choice of the metal catalyst is of prime importance. For this redox reaction to occur, the catalyst needs to be more electronegative than Si so that electrons are attracted away from Si atoms and the oxidation of Si is expedited.[21] The metal will also need to be inert to both H_2O_2 and HF to enable long etching duration in forming nanowires. Au and Ag are excellent choices based on the above requirements. As opposed to having a metal that has a higher electronegativity than Si, using a less electronegative metal will understandably result in limited Si oxidation since the metal itself will be preferably oxidized when in contact with an oxidizing agent. Therefore, metals like chromium (Cr) (less electronegative than Si), can be an effective blocking layer for the catalytic etching, and this will be demonstrated. It is equally important to prevent the oxidation and etching of Cr, and this can be achieved by capping the Cr with an inert layer of Au. The masking property of Cr/Au for Au-assisted catalytic etching was indeed clearly demonstrated in a simple control experiment using micrometer-sized Cr/Au markers (see Supporting Information).

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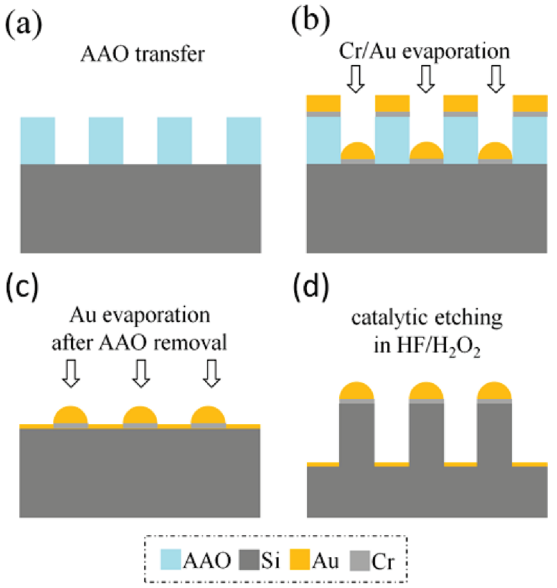

Figure 1. Schematic of the SiNW fabrication process. (a) AAO membrane is transferred onto the surface of a Si substrate. (b) Evaporation of Cr/Au nanodots through the AAO pores forming the blocking metal nanodots on Si. (c) Removal of the AAO template before the subsequent deposition of a thin Au layer that will act as the etching catalyst. (d) Anisotropic etching and formation of SiNWs by immersing the sample in HF/H_2O_2.

The fabrication procedure for SiNW fabrication employed in this work is schematically illustrated in Figure 1. An ultrathin AAO membrane was first transferred to the surface of a Si (100) wafer (p-type, resistivity of 4 to 8 Ω-cm) that was precleaned by sonication in acetone and then in isopropyl alcohol (IPA), for a duration of 15 min each. The detailed procedure of the AAO fabrication and its transfer to a Si surface can be found in ref 31. Unlike the templated VLS growth of SiNWs discussed earlier, any HF etching of the native oxide on the wafer surface is not necessary since the catalytic etching is not affected by the presence of the thin oxide layer.[32] Subsequently, 10 nm of Cr, followed by 30 nm of Au, was thermally evaporated through AAO pores onto the Si surface to produce regular arrays of Cr/Au metallic nanodots. The AAO template was then removed, and a thin layer of Au of 7 nm was evaporated on the sample surface. Both the evaporation of the metal dots and the Au catalyst film were achieved using an Edwards Auto 306 evaporator with a base pressure of $\sim 3.0 \times 10^{-7}$ mbar. The deposition thickness was monitored in situ by a quartz crystal microbalance (QCM). The chemical wet etching in a dark environment was carried out in a solution consisting of 4.6 M HF and 0.44 M H_2O_2 for durations of 30 s to 3 min, depending on the length of the nanowires required. After the etching process, the sample was rinsed in DI water and dried in an oven at 90 °C.

Results and Discussion

Figure 2a shows the scanning electron microscopy (SEM) (Jeol Nova NanoSem 230) image of a typical AAO template (with pores widened) used in our experiments, with a higher magnification image shown in the inset. The corresponding high density Cr/Au metal dots produced are depicted in Figure 2b. These two SEM micrographs show that the size and the ordering of the metal dots closely match with that of the AAO template indicating that the masking deposition is successful with little or no shadowing effects. The SEM image of the etched SiNWs obtained at an oblique angle is shown in Figure 2c while a top view of the nanowires is shown in Figure 2d. The higher magnification SEM image in the inset in Figure 2c shows the presence of the Cr/Au tips, demonstrating the blocking effect of the metal nanodots. From our numerous SEM micrographs, we estimate the average wire density to be 6×10^7 mm^{-2}, which is higher than the previously reported densities using laser interference lithography and nanosphere lithography.[24−26] The improvement in the wire density represents a tremendous opportunity in improving the performance of devices such as sensors, light emitting diodes or photovoltaics, whereby a high density array is greatly desired. The average diameter of the SiNWs shown in Figure 2 is about 70 nm although other values can be achieved as will be subsequently shown. The SEM images of the SiNWs also show a good match of the wire arrangement with the nanodots and hence the AAO. Since the size of the as-synthesized nanowire depends strongly on the diameter of the masking Cr/Au dots, the size distribution of SiNWs diameters was examined for comparison with the sizes of the Cr/Au dots. The distribution frequency histograms of 100 individual Cr/Au dots and SiNWs are shown in Figure 3. The Gaussian fit shows that the mean diameter and the standard deviation of the wires closely match with those of the masking Cr/Au dots. This is an indication that there was no surface migration of the metal nanodots during the etching process. The highly anisotropic etching is also clearly demonstrated as we only observe orthogonal (to the Si wafer surface) SiNWs from our fabrication process.

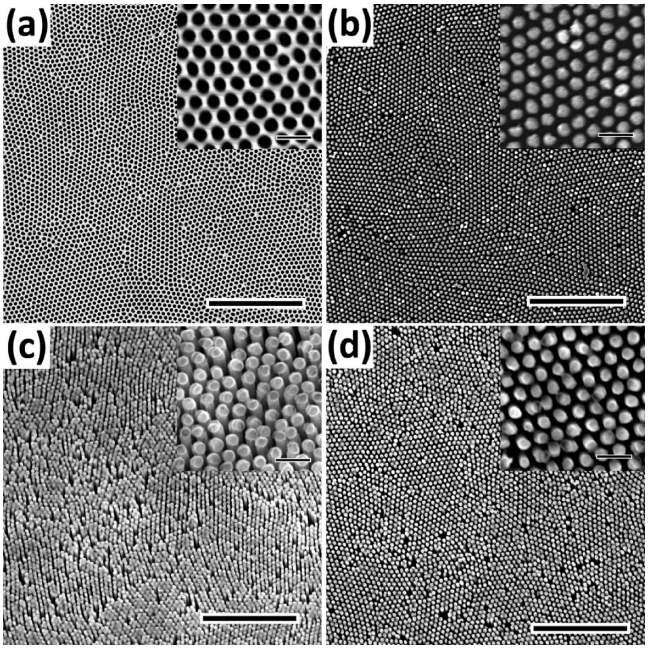

Figure 2. (a) SEM micrograph of a pore-widened AAO membrane and (b) the corresponding Cr/Au nanodots deposited through the AAO membrane onto Si (100). SEM images of etched SiNWs taken at (c) a 30°-tilt view (tilt angle from the normal) and (d) a 0°-tilt view. Higher-magnification images of all SEM images are shown in their respective insets. The scale bars are 2 μm for all the micrographs and 200 nm for all the insets.

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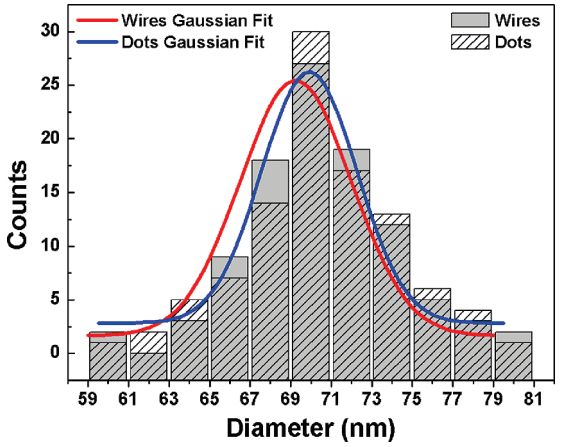

Figure 3. Size distributions of 100 individual masking Cr/Au dots and SiNWs for the case of using an AAO with an average pore size of ~70 nm. The Gaussian fit shows that the wires have a mean diameter of 69.1 nm and a standard deviation of 3.9 nm, which are closely matched with the mean diameter (70.0 nm) and the standard deviation (3.3 nm) of the masking Cr/Au dots.

There is also a good correlation of the length of the wires and the duration of the chemical etch, with an estimated etch rate of ~1 μm per minute (Figures 4a to 4c). The etch rate was found to be similar and showed negligible dependence on the wire diameters and spacings (fabrication of SiNWs of different diameters and spacings will be discussed later). This is an advantage over both the VLS and the DRIE processes that are feature size and spacing dependent. For DRIE, small wire diameters or spacings can lead to non-uniform etch depths (hence wire lengths) or branching that can be pronounced for high aspect ratios wires with small feature sizes.[19] For the VLS wires, controlling the wire length can be complicated for a SiNW sample with different wire diameters and spacings.[33] In our work that uses catalytic etching, the wire length is basically a function of the etch duration regardless of the wire diameter and spacing as shown by the similar etch rates for different diameters. In other words, the aspect ratio can be tuned by strictly controlling the pore size of the AAO template and, more importantly, the etch duration. We have achieved wires with aspect ratios of >40 although a higher ratio is possible since the maximal achievable aspect ratio is only limited by the eventual dissolution of the nanowires in the etching solution,[25] a process that is much slower than the dissolution of the catalyst-covered silicon. We add that aspect ratios as high as 220 have been previously reported.[23] We note that in some rare cases, the metal nanodots may be detached from the top of the wire as represented in Figure 4b. This is probably a consequence of the rinsing/drying process since the wires formed are still of similar length and diameter. This therefore, imposes no problem to the fabrication of the SiNWs. Interestingly, for longer nanowires (Figure 4c), we observe a loss of the vertical alignment between the wires that is not uncommon for high density of long SiNWs.[23,34] We believe that this could be a result of surface tension in the drying process after the DI water rinse, which can possibly be avoided using critical point drying.[23]

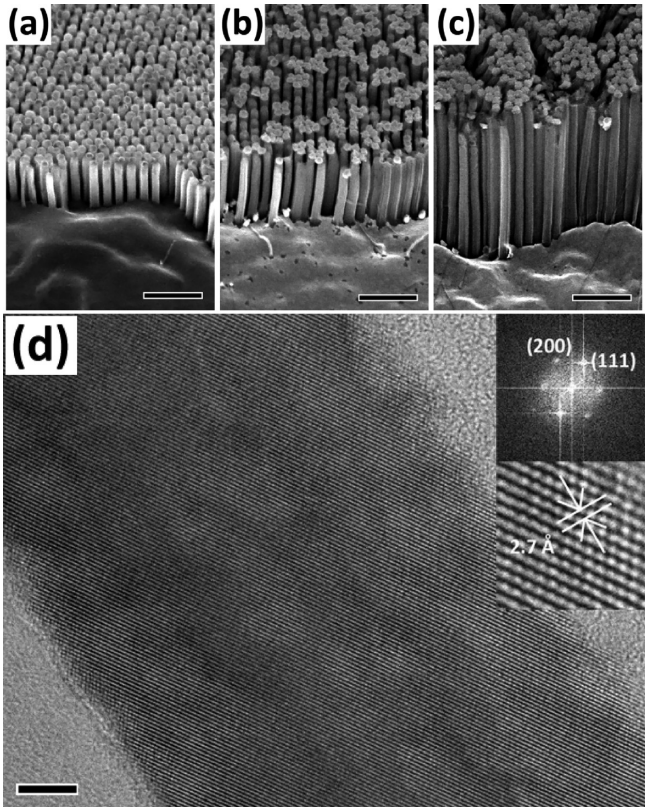

Figure 4. SEM images taken at a 45°-tilt view of the SiNWs fabricated after immersion in the etching solution for (a) 30 s, (b) 60 s, and (c) 120 s. Scale bars are 500 nm for all the SEM images. (d) TEM image of a typical SiNW. Well-defined lattice fringes are clearly observed throughout the wire. The insets are the FFT pattern of the SiNW and the TEM image of the Si lattice at a higher magnification. Both insets show the ⟨100⟩ axial orientation of the wire. The scale bar for the TEM image is 5 nm.

To study the crystallinity of the etched SiNWs, high resolution transmission electron microscopy (HRTEM) characterization (Jeol JEM 2100) was carried out. TEM samples were prepared by sonication of the etched samples in ethanol for 15 min. The wires were then suspended in ethanol and transferred to a carbon−copper grid for the TEM analysis. Figure 4d shows the HRTEM image of a single nanowire with a diameter of 40 nm. Well-defined fringes are observed across the entire wire indicating that the wire is single crystalline. The average spacing between two adjacent planes in the axial direction is found to be 2.7 Å that corresponds to the ⟨001⟩ direction. This axial orientation was further verified by the Fast Fourier Transform (FFT) analysis of the HRTEM image as shown in the inset in Figure 4d. The ⟨001⟩ direction of the SiNW is a confirmation of the vertical and anisotropic etching as discussed. The SiNW shown in the TEM image has a relatively smooth surface. Since the surface roughness of SiNWs prepared by metal-assisted chemical etching can increase with etching time, because of the random isotropic etching of Si by the etching solution (sidewall etching

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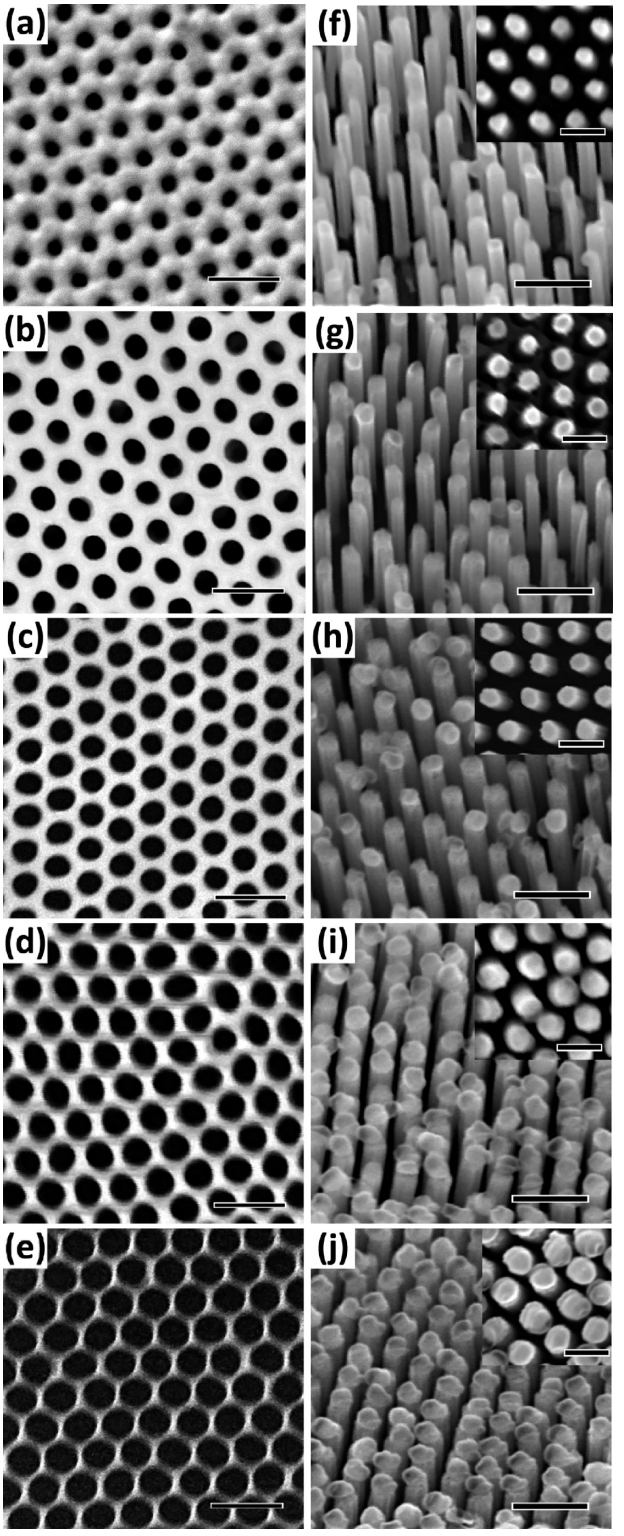

Figure 5. SEM images of AAOs with average pore diameters of (a) 40 nm, (b) 50 nm, (c) 60 nm, (d) 70 nm, and (e) 80 nm. The corresponding SiNWs produced using these AAO templates are shown in panels (f) to (j), respectively. The insets of each image are the respective top-view SEM images of the SiNWs shown in the micrograph. The mean diameters and the standard deviations, in nanometers (nm), are (41.3, 4.4), (49.7, 3.7), (60.5, 4.3), (69.1, 3.9), and (80.2, 3.3), respectively. Scale bars are 200 nm for all SEM images and 100 nm for all the insets.

without the Au catalyst), the surface roughness (< 2 nm root-mean-square) we obtained is reasonable given the relatively long etching time of 2 min.

We have thus demonstrated for the first time the ability to use an AAO-patterned metal nanodot array as a masking template in etching SiNWs. This is of tremendous value since a careful manipulation of the pore size of the AAO template will allow one to have control over the diameter of the nanowires. One convenient way to achieve this is to subject the as-fabricated AAO membrane to an extra pore widening process in a dilute acid or alkali solution. By immersing the AAO into a 5% wt. phosphoric acid, which gives an approximate etch rate of 10 nm per 10 min or 1 nm/minute, we can fine-tune the pore size, ranging from an initial pore diameter of 40 nm to a widened pore size of up to 80 nm, depending on the widening immersion duration. These AAO membranes can then be employed in the same fabrication procedure as described to produce SiNWs of high density with uniform diameters. Figure 5a to 5e are the SEM images of AAO membranes with pore sizes from 40 to 80 nm in steps of 10 nm. The corresponding SiNWs produced using these templates are shown in Figures 5f to 5j. Given the slow rate of pore widening, a finer step change of less than 10 nm can be readily achieved, though this is not demonstrated for the present work. While the lower bound of the SiNW diameter is set by the initial pore size of the starting AAO fabricated (~40 nm for an oxalic acid anodization process), the maximum value of the nanowire diameter is limited by the interpore spacing (~90 nm in this work). We have also tested on less regular arrays of AAO and concluded that the Cr/Au masking can achieve feature size of sub-20 nm. In addition, it should be noted that AAO with different pore diameters and interpore distances can be produced using different electrolytes and anodic potentials in the anodization process.[35] This offers even greater flexibility in the control of the diameter range that will be of great value and interest for device applications. Furthermore, wafer-scale AAO templates can also be directly fabricated on a Si wafer through utilization of a laser interference or nanoimprint technique,[36,37] allowing a convenient way of wafer-scale production of SiNWs using our approach. Lastly and also most importantly, our method, as demonstrated in the Cr/Au marker control experiment (see Supporting Information), is generic. The formation of Cr/Au masking regions are thus not limited to just AAO templates and can be patterned by other common lithography techniques. This opens up a whole new window for Si nanostructures with small feature sizes and complicated design patterns that can be of great importance for Si-based nano devices.

Conclusion

In conclusion, we have developed a simple and low-cost method to fabricate high-density and well-aligned SiNWs through metal-assisted chemical etching using metal nanodots

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as a hard mask. By fine-tuning the pore size of the AAO template used in the metal nanodot fabrication, we can precisely control the diameter of SiNWs down to a precision of 10 nm in the range of 40 to 80 nm. The use of Cr/Au as a hard mask blocking material will also be of tremendous value for other patterning methods for Si nanostructure fabrication using catalytic etching.

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Supporting Information Available: Further details on the verification of Cr/Au masking properties for Au-assisted catalytic etching. This material is available free of charge via the Internet at http://pubs.acs.org.